PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8725
1-TO-5
DIFFERENTIAL-TO-LVHSTL ZERO DELAY BUFFER

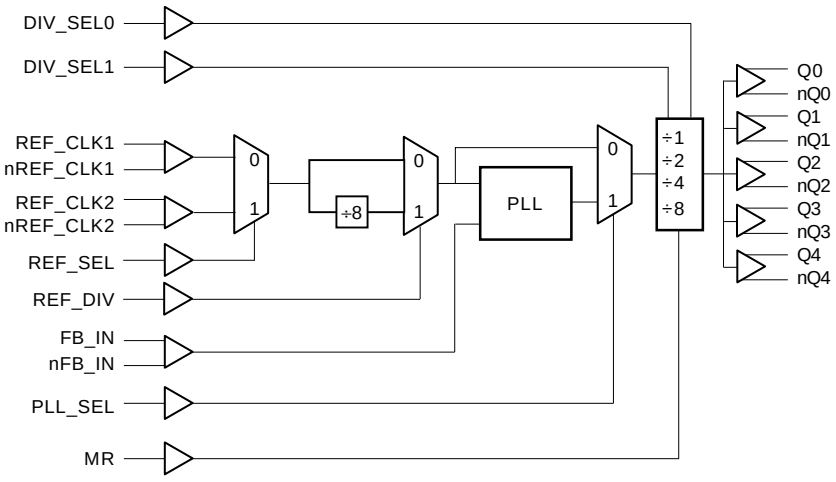
GENERAL DESCRIPTION

The ICS8725 is a high performance LVHSTL zero delay buffer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The VCO operates at a frequency range of 250MHz to 500MHz. Utilizing one of the outputs as feedback to the PLL output frequencies up to 500MHz can be regenerated with zero delay with respect to the input. Dual reference clock inputs support redundant clock or multiple reference applications.

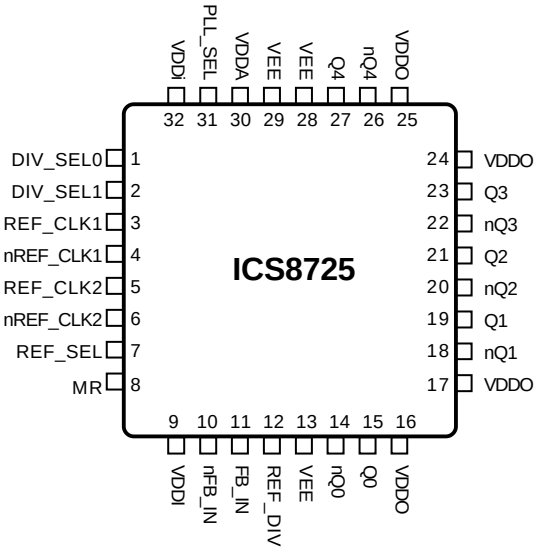
FEATURES

- Fully integrated PLL
- 5 LVHSTL outputs each with the ability to drive 50Ω to ground
- Voh (max) = 1.2V
- 31.25MHz to 500MHz output frequency range
- Spread Smart™ for regenerating spread spectrum clocks
- Differential reference clock inputs accept any differential input signal
- Differential reference clock inputs will accept single ended input signal with one of the inputs biased with a resistor network
- 31.25MHz to 622MHz input frequency range
- LVCMOS / LVTTL control inputs
- 3.3V core, 1.8V output operating supply voltage
- 32 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.8mm package lead pitch
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	DIV_SEL0	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTL interface levels.
2	DIV_SEL1	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTL interface levels.
3	REF_CLK1	Input	Pulldown	Non-inverting differential clock input.
4	nREF_CLK1	Input	Pullup	Inverting differential clock input.
5	REF_CLK2	Input	Pulldown	Non-inverting differential clock input.
6	nRE2_CLK2	Input	Pullup	Inverting differential clock input.
7	REF_SEL	Input	Pulldown	Differential clock select input. When Low selects REF_CLK2 or nREF_CLK2. When HIGH selects REF_CLK1 or nREF_CLK1.
8	MR	Input	Pulldown	Resets dividers and determine state of the outputs. LVCMOS / LVTTL interface levels.
9	VDDI	Power		Input and core power supply pin. Connect to 3.3V.
10	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
11	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
12	REF_DIV	Input	Pulldown	
13, 28, 29	VEE	Power		Ground pins. Connect to ground.
14, 15	nQ0, Q0	Output		Differential clock outputs. 50Ω typical output impedance. LVHSTL interface levels.
16. 17, 24, 25	VDDO	Power		Output power supply pins. Connect to 1.8V.
18, 19	nQ1, Q1	Output		Differential clock outputs. 50Ω typical output impedance. LVHSTL interface levels.
20, 21	nQ2, Q2	Output		Differential clock outputs. 50Ω typical output impedance. LVHSTL interface levels.
22, 23	nQ3, Q3	Output		Differential clock outputs. 50Ω typical output impedance. LVHSTL interface levels.
26, 27	nQ4, Q4	Output		Differential clock outputs. 50Ω typical output impedance. LVHSTL interface levels.
30	VDDA	Power		PLL power supply pin. Connect to 3.3V.
31	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH select PLL. When LOW selects reference clock. LVCMOS / LVTTL interface levels.
32	VDDI	Power		Output power supply pin. Connect to 3.3V.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	REF_CLK1, nREF_CLK1, REF_CLK2, nREF_CLK2, FB_IN, nFB_IN			TBD		pF
		DIV_SEL0, DIV_SEL1, REF_SEL, REF_DIV PLL_SEL, MR			TBD		pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3. CONTROL INPUTS FUNCTION TABLE

DIV_SEL1	DIV_SEL0	FREQUENCY (MHz)	
		MINIMUM	MAXIMUM
0	0	250	250
0	1	125	250
1	0	62.5	125
1	1	31.25	62.5

TABLE 4. PLL INPUT REFERENCE CHARACTERISTICS, VDDI=VDDA=3.3V±5%, VDDO=1.8V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fREF	Input Reference Frequency		20		250	MHz
tR	Input Rise Time	Measured at 20% to 80% points			TBD	ns
tF	Input Fall Time	Measured at 20% to 80% point			TBD	ns
tDC	Input Reference Duty Cycle		TBD		TBD	%

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, VDDI=VDDA=3.3V±5%, VDDO=1.8V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage			1.8		V
IEE	Power Supply Current					mA

TABLE 5B. DIFFERENTIAL DC CHARACTERISTICS, VDDI=VDDA=3.3V±5%, VDDO=1.8V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	REF_CLK1, REF_CLK2, FB_IN	VIN = 3.465V			150	µA
		nREF_CLK1, nREF_CLK2, nFB_IN	VIN = 3.465V			5	µA
IIL	Input Low Current	REF_CLK1, REF_CLK2, FB_IN	VIN = 0V	-5			µA
		nREF1, nREF2, nFB_IN	VIN = 0V	-150			µA

NOTE: For REF_CLK1, nREF_CLK1 and REF_CLK2, nREF_CLK2 input levels, see VPP and VCMR in AC Characteristics table.

TABLE 5C. LVCMOS DC CHARACTERISTICS, VDDI=VDDA=3.3V±5%, VDDO=1.8V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	DIV_SEL0, DIV_SEL1, REF_SEL, PLL_SEL, REF_DIV, MR		2		3.765	V
VIL	Input Low Voltage	DIV_SEL0, DIV_SEL1, REF_SEL, PLL_SEL, REF_DIV, MR		-0.3		0.8	V
IIH	Input High Current	DIV_SEL0, DIV_ SEL1, REF_DIV, REF_SEL, MR	VIN = 3.465V			150	µA
		PLL_SEL	VIN = 3.465V			5	µA
IIL	Input Low Current	DIV_SEL0, DIV_ SEL1, REF_DIV, REF_SEL, MR	VIN = 0V	-5			µA
		PLL_SEL	VIN = 0V	-150			µA

TABLE 5D. LVHSTL DC CHARACTERISTICS, VDDI=VDDA=3.3V±5%, VDDO=1.8V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		1.0		1.2	V
VOL	Output Low Voltage; NOTE 1		0		0.4	V
VOX	Output Crossover Voltage		40% x (VOH-VOL) + VOL		60% x (VOH-VOL) + VOL	V

NOTE 1: Outputs terminated with 50Ω to ground. The power dissipation of a terminated output pair is 32mW.

TABLE 6. AC CHARACTERISTICS, VDDI=VDDA=3.3V±5%, VDDO=1.8V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Output Frequency					500	MHz
VPP	Peak-to-Peak Input Voltage		f = 500MHz				
VCMR	Common Mode Input Voltage		f = 500MHz				
tpLH	Propagation Delay, Low-to-High		PLL_SEL=0V, 0MHz ≤ f ≤ 500MHz	TBD		TBD	ns
tpHL	Propagation Delay, High-to-Low		PLL_SEL=0V, 0MHz ≤ f ≤ 500MHz	TBD		TBD	ns
t(Ø)	PLL Reference Zero Delay; NOTE 2	REF_CLK1, nREF_CLK1 REF_CLK2, nREF_CLK2	PLL_SEL=3.3V, fREF=TBD, fVCO=TBD	-100	TBD	100	ps
tsk(o)	Output Skew; NOTE 3		Measured on rising edge at VDDO/2			100	ps
tjit(cc)	Cycle-to-Cycle Jitter		Measured on rising edge at VDDO/2		±100		ps
tL	PLL Lock Time					TBD	
tR	Output Rise Time			TBD		TBD	ps
tF	Output Fall Time			TBD		TBD	ps
tPW	Output Pulse Width		0MHz ≤ f ≤ 500MHz	tCYCLE/2 -TBD	tCYCLE/2	tCYCLE/2 +TBD	ns
			f = 500MHz	TBD	2.08	TBD	ns
tEN	Output Enable Time					TBD	ns
tDIS	Output Disable Time					TBD	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent pairs of cycles.

PACKAGE OUTLINE - Y SUFFIX

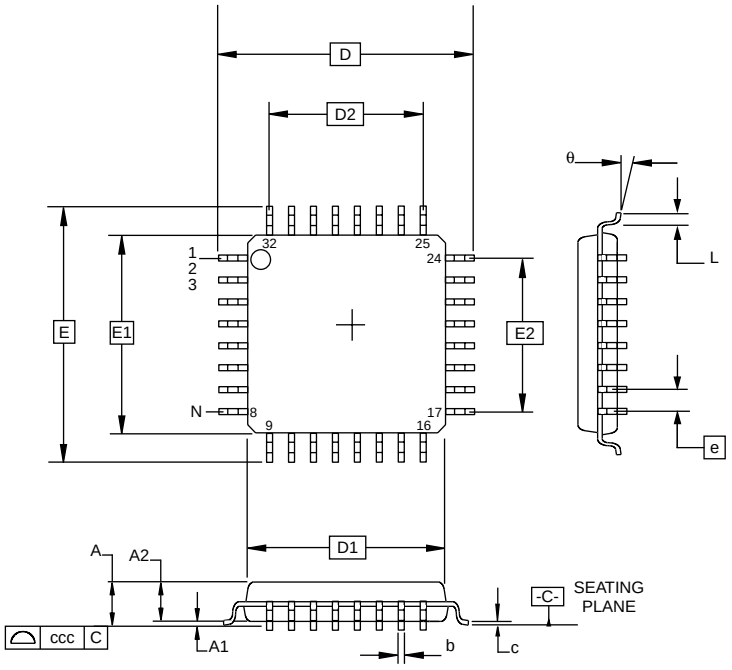


TABLE 7. PACKAGE DIMENISIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8725Y	ICS87251	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8725YT	ICS8725	32 Lead LQFP on Tape and Reel	2000	0°C to 70°C